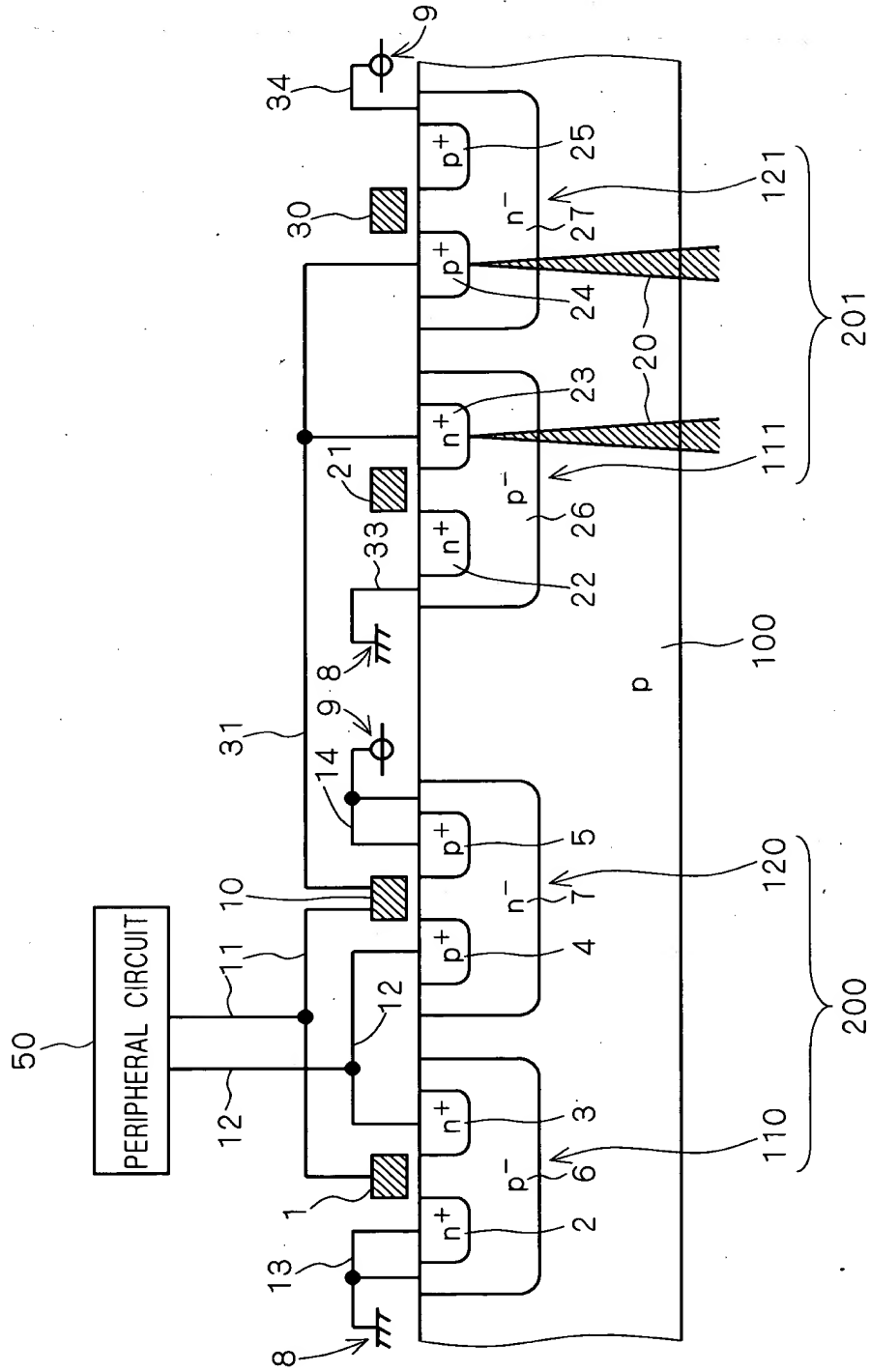


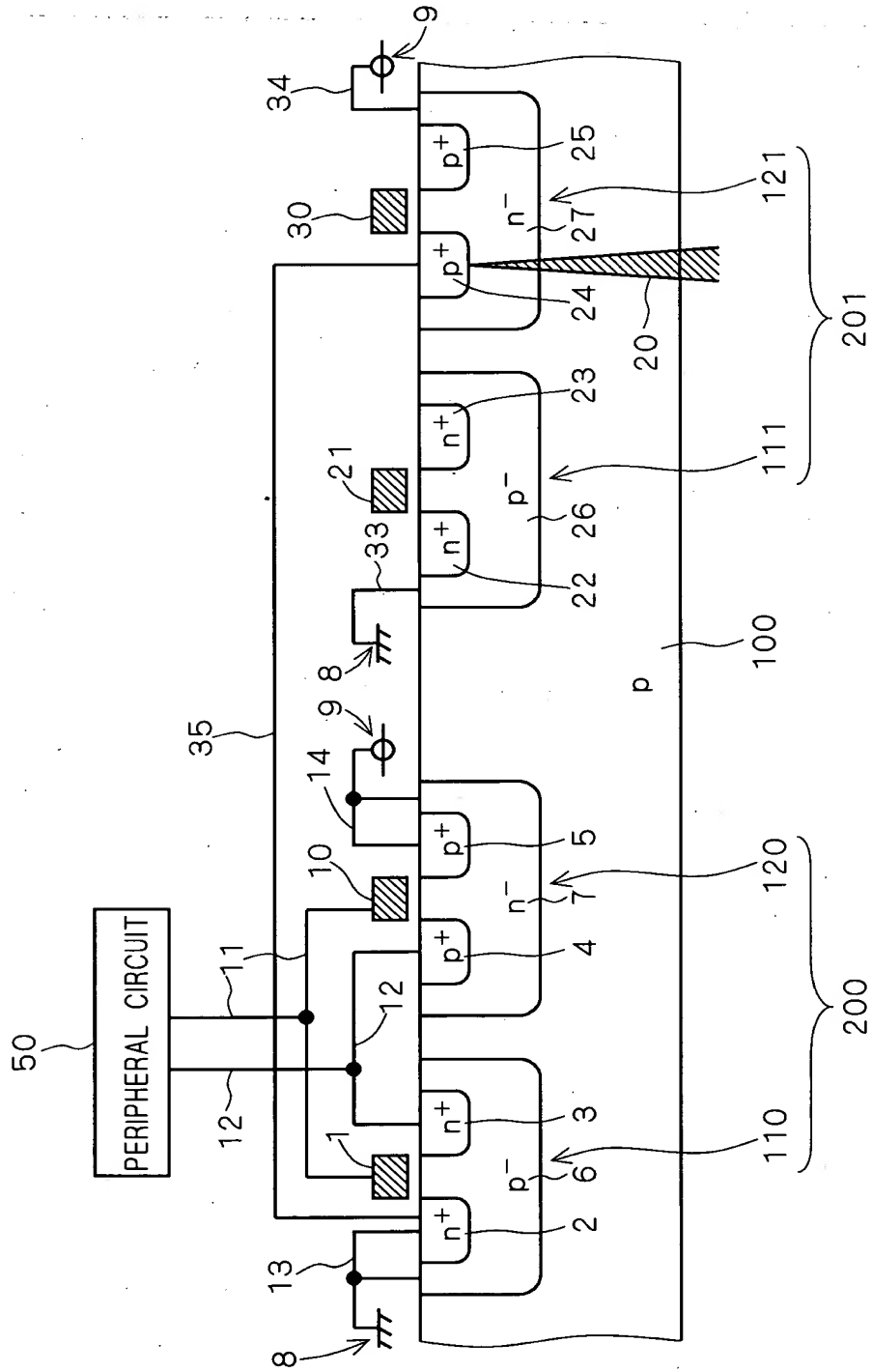
FIG. 1



This diagram shows a cross-sectional view of a semiconductor device. A substrate 100 is divided into a peripheral circuit region 200 and a main circuit region 201. The peripheral circuit region 200 contains a peripheral circuit 50, which includes a series of transistors 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50. The main circuit region 201 contains a main circuit 100, which includes a series of transistors 110, 120, 130, 140, 150, 160, 170, 180, 190, 200, 210, 220, 230, 240, 250, 260, 270, 280, 290, 300, 310, 320, 330, 340, 350, 360, 370, 380, 390, 400, 410, 420, 430, 440, 450, 460, 470, 480, 490, 500. The device is formed on a substrate 100, which is divided into a peripheral circuit region 200 and a main circuit region 201. The peripheral circuit region 200 contains a peripheral circuit 50, which includes a series of transistors 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50. The main circuit region 201 contains a main circuit 100, which includes a series of transistors 110, 120, 130, 140, 150, 160, 170, 180, 190, 200, 210, 220, 230, 240, 250, 260, 270, 280, 290, 300, 310, 320, 330, 340, 350, 360, 370, 380, 390, 400, 410, 420, 430, 440, 450, 460, 470, 480, 490, 500.

This diagram shows a cross-sectional view of a semiconductor device. A substrate 100 is divided into a peripheral circuit region 200 and a memory array region 201. In the peripheral circuit region 200, a peripheral circuit 50 is formed on the surface, including a gate stack 12, a source/drain region 11, and a contact 10. The memory array region 201 contains a series of memory cells. Each memory cell consists of a gate stack 20, a source/drain region 21, and a contact 22. The gate stack 20 is formed on a p-type substrate 100, with n+ regions 23 and p- regions 24. The source/drain region 21 is formed on a p-type substrate 100, with n+ regions 25 and p- regions 26. The contact 22 is formed on a p-type substrate 100, with n+ regions 27 and p- regions 28. The peripheral circuit 50 is connected to the memory array region 201 via a contact 14 and a gate stack 12.

FIG. 4



This diagram shows a cross-sectional view of a semiconductor device. A peripheral circuit (50) is located on the left, containing a PERIPHERAL CIRCUIT block (60) and a series of transistors (1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14). These transistors are connected to a word line (12) and a bit line (41). The main array (200) consists of a grid of memory cells (110, 120, 121) formed by intersecting word lines and bit lines. The device is built on a p-type substrate (100) and includes various doped regions (n+, n-, p+, p-) and insulating layers (20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34). A gate stack (9) is shown on top of the array.

F / G. 6

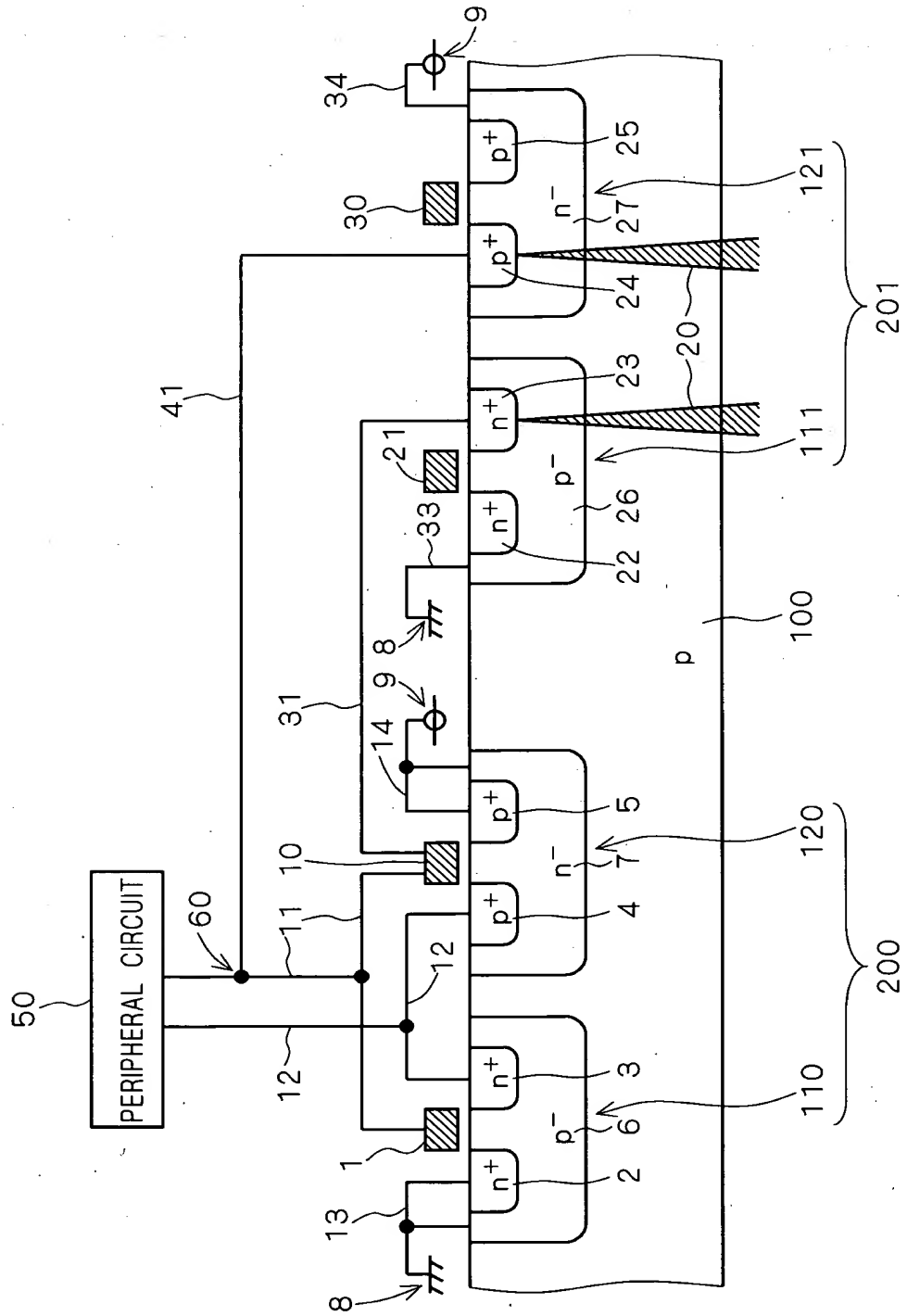


FIG. 7

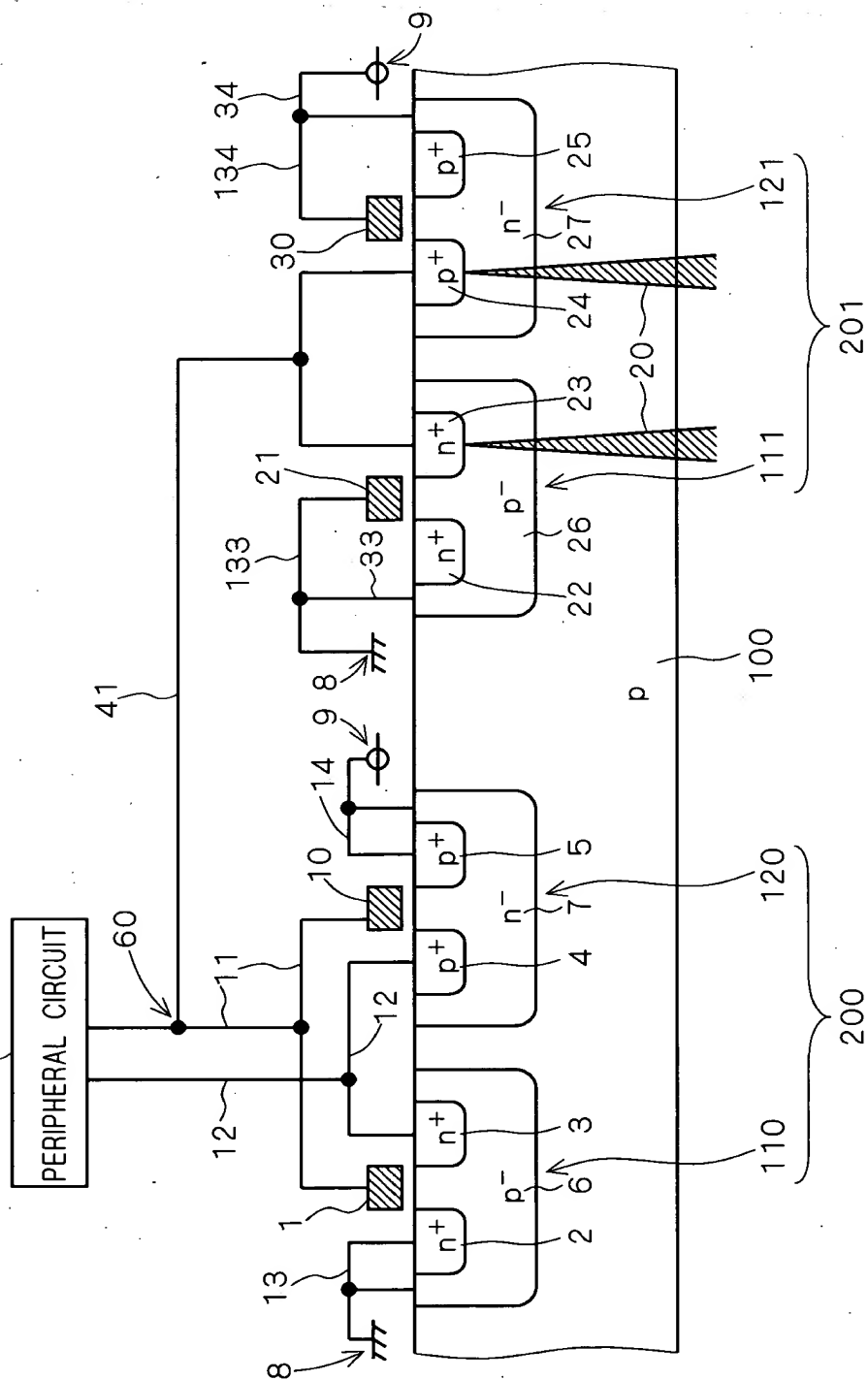
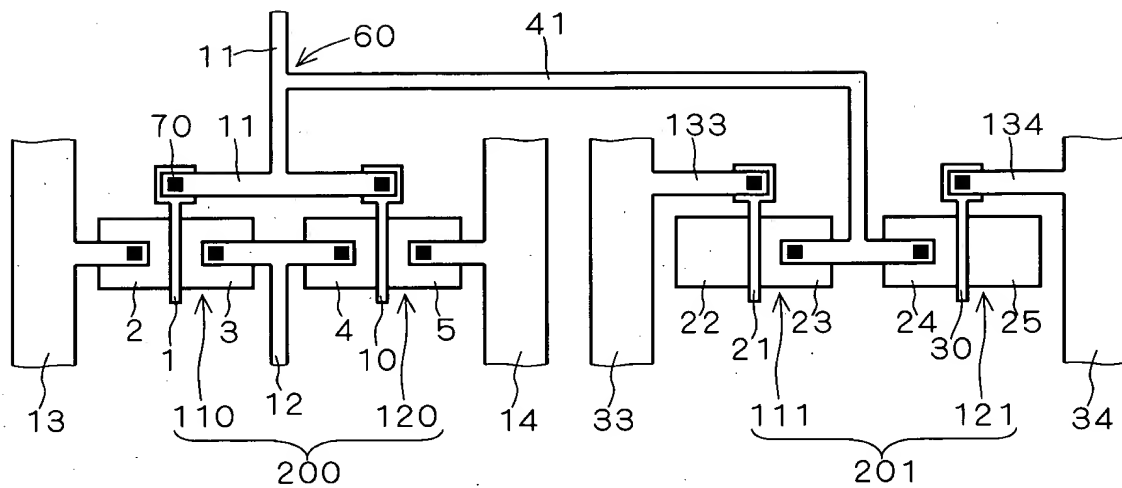


FIG. 8



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FIG. 9A

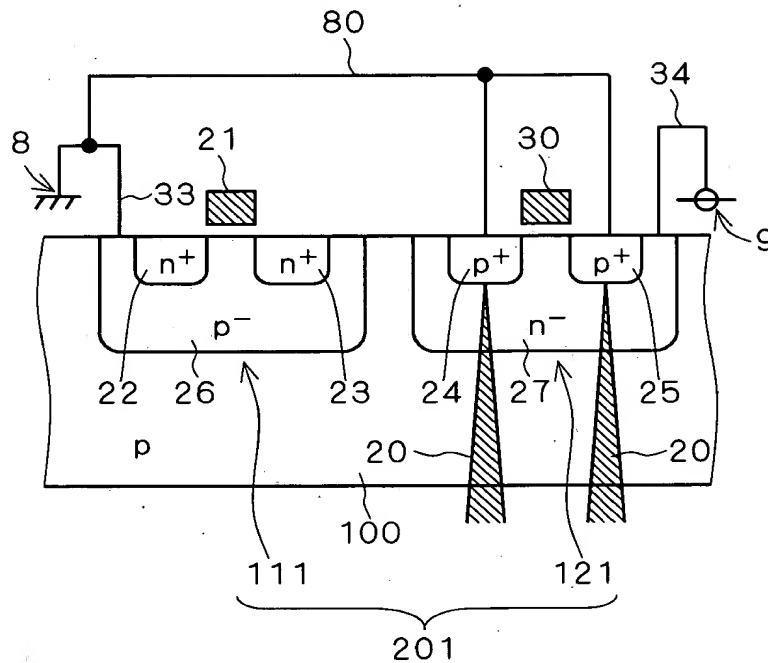
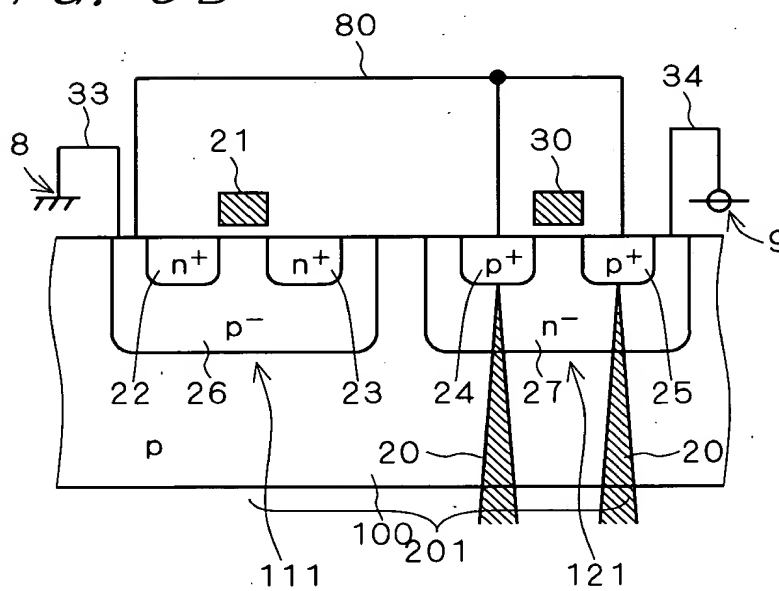


FIG. 9B



$F / G. \quad 10B$

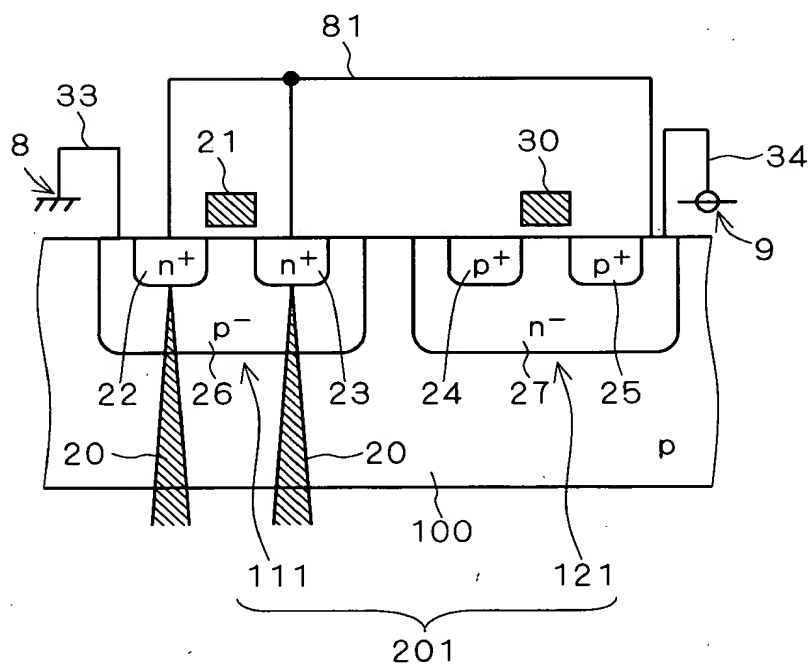
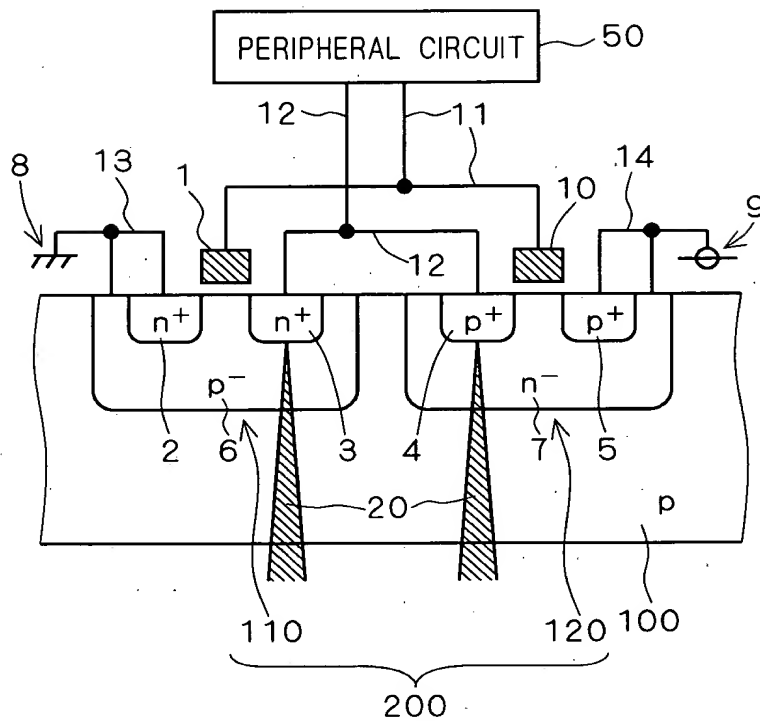


FIG. 11



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